



ISO/IEC 14165-122

Edition 2.1 2008-11  
CONSOLIDATED VERSION

# INTERNATIONAL STANDARD

---

**Information technology – Fibre channel –  
Part 122: Arbitrated loop-2 (FC-AL-2)**

INTERNATIONAL  
ELECTROTECHNICAL  
COMMISSION

---

ICS 35.200

ISBN 2-8318-9775-0

**Warning! Make sure that you obtained this publication from an authorized distributor.**

## CONTENTS

|  |    |
|--|----|
| FOREWORD.....  | 8  |
| INTRODUCTION.....  | 10 |
| 1 Scope .....  | 12 |
| 2 Normative references .....                             | 12 |
| 3 Definitions and conventions.....                       | 13 |
| 3.1 Definitions .....                                    | 13 |
| 3.2 Editorial conventions .....                          | 16 |
| 3.3 Abbreviations, acronyms and other special words..... | 16 |
| 3.4 Symbols .....  | 19 |
| 4 Structure and concepts.....                            | 19 |
| 4.0 Purpose.....   | 19 |
| 4.1 Overview .....                                       | 19 |
| 4.2 General description.....                             | 20 |
| 4.3 Access fairness algorithm .....                      | 22 |
| 4.3.0 Access fairness overview .....                     | 22 |
| 4.3.1 Access fairness for NL_Ports.....                  | 22 |
| 4.3.2 Access unfairness for NL_Ports.....                | 22 |
| 4.3.3 Access unfairness for FL_Ports .....               | 23 |
| 4.4 Relationship to FC-PH .....                          | 23 |
| 5 Addressing.....  | 25 |
| 5.1 Arbitrated Loop Physical Address (AL_PA).....        | 25 |
| 5.1.1 Valid AL_PAs .....                                 | 27 |
| 5.1.2 Special AL_PAs and flags.....                      | 27 |
| 5.2 Native address identifier .....                      | 27 |
| 6 FC-AL Ordered Sets.....                                | 28 |
| 7 FC-AL Primitive Signals and Sequences.....             | 29 |
| 7.0 Overview .....                                       | 29 |
| 7.1 Arbitrate Primitive Signals (ARByx).....             | 29 |
| 7.1.0 ARByx overview .....                               | 29 |
| 7.1.1 ARB(AL_PA) .....                                   | 29 |
| 7.1.2 ARB(F0).....                                       | 29 |
| 7.1.3 ARB(FF).....                                       | 30 |
| 7.2 Open Primitive Signals (OPNy).....                   | 30 |
| 7.2.0 OPNy overview.....                                 | 30 |
| 7.2.1 Open full-duplex (OPNyx).....                      | 30 |
| 7.2.2 Open half-duplex (OPNyy).....                      | 30 |
| 7.3 Open Replicate Primitive Signals (OPNr).....         | 31 |
| 7.3.0 OPNr overview .....                                | 31 |
| 7.3.1 Open selective replicate (OPNyr).....              | 31 |
| 7.3.2 Open broadcast replicate (OPNfr).....              | 31 |
| 7.4 Close Primitive Signal (CLS).....                    | 32 |
| 7.5 Dynamic Half-Duplex Primitive Signal (DHD) .....     | 32 |
| 7.6 Mark Primitive Signal (MRKtx) .....                  | 32 |
| 7.7 Loop Port Bypass/Enable Primitive Sequences .....    | 33 |

|         |  |    |
|---------|--|----|
| 7.7.0   | LPE/LPB overview .....                                       | 33 |
| 7.7.1   | Loop Port Bypass (LPByx) .....                               | 33 |
| 7.7.2   | Loop Port Bypass all (LPBfx) .....                           | 34 |
| 7.7.3   | Loop Port Enable (LPEyx) .....                               | 34 |
| 7.7.4   | Loop Port Enable all (LPEfx) .....                           | 34 |
| 7.8     | Loop initialization primitive sequences (LIP) .....          | 35 |
| 7.8.0   | LIP overview .....   | 35 |
| 7.8.1   | Loop Initialization — no valid AL_PA .....                   | 35 |
| 7.8.2   | Loop Initialization — Loop Failure; no valid AL_PA .....     | 35 |
| 7.8.3   | Loop Initialization — valid AL_PA .....                      | 35 |
| 7.8.4   | Loop Initialization — Loop Failure; valid AL_ .....          | 35 |
| 7.8.5   | Loop Initialization — reset L_Port .....                     | 35 |
| 7.8.6   | Loop Initialization — reserved .....                         | 35 |
| 8       | L_Port operation .....                                       | 36 |
| 8.0     | Overview .....   | 36 |
| 8.1     | History .....  | 36 |
| 8.1.1   | Access fairness history .....                                | 36 |
| 8.1.2   | Duplex mode history .....                                    | 37 |
| 8.1.3   | Replicate mode history .....                                 | 37 |
| 8.1.4   | Operational mode history .....                               | 37 |
| 8.1.5   | DHD received history .....                                   | 38 |
| 8.1.6   | ARB(FF) history .....  | 38 |
| 8.2     | Timeouts .....   | 38 |
| 8.2.1   | FC-PH timeout values .....                                   | 38 |
| 8.2.2   | Arbitrated Loop timeout value .....                          | 38 |
| 8.2.3   | Loop timeout .....   | 39 |
| 8.3     | Operational characteristics .....                            | 39 |
| 8.3.1   | Transmission Word .....                                      | 39 |
| 8.3.1.1 | Power-on Transmission Words .....                            | 39 |
| 8.3.1.2 | Invalid Transmission Words and Transmission Characters ..... | 39 |
| 8.3.2   | Clock skew management .....                                  | 39 |
| 8.3.3   | Error detection and recovery .....                           | 40 |
| 8.3.4   | BB_Credit and Available_BB_Credit .....                      | 40 |
| 8.3.4.0 | BB_Credit overview .....                                     | 40 |
| 8.3.4.1 | BB_Credit management per Loop circuit .....                  | 41 |
| 8.3.4.2 | Available_BB_Credit management per Loop .....                | 42 |
| 8.4     | Loop Port State Machine (LPSM) .....                         | 42 |
| 8.4.0   | LPSM overview .....  | 42 |
| 8.4.1   | State names .....  | 42 |
| 8.4.2   | State diagram .....  | 43 |
| 8.4.3   | Reference items .....  | 45 |
| 9       | L_Port state transition tables .....                         | 61 |
| 10      | Loop Initialization procedure .....                          | 86 |
| 10.0    | Loop Initialization overview .....                           | 86 |
| 10.1    | Loop Initialization summary .....                            | 86 |
| 10.2    | Loop Initialization introduction .....                       | 87 |
| 10.3    | Loop Initialization timers .....                             | 87 |

|                       |  |     |
|-----------------------|--|-----|
| 10.4                  | Node-initiated L_Port initialization .....                 | 88  |
| 10.5                  | L_Port initialization .....                                | 88  |
| 10.5.0                | Initialization overview .....                              | 88  |
| 10.5.1                | Loop Initialization Sequences .....                        | 89  |
| 10.5.2                | Assigned AL_PA values.....                                 | 90  |
| 10.5.3                | Loop Initialization steps .....                            | 92  |
| 10.5.4                | Loop Initialization state diagram .....                    | 96  |
| 10.5.4.0              | State diagram overview .....                               | 96  |
| 10.5.4.1              | Validity of AL_PA.....                                     | 98  |
| 10.5.4.2              | POWER-ON state diagram .....                               | 100 |
| 10.5.4.3              | OLD-PORT state diagram .....                               | 101 |
| 10.5.4.5              | Normal Initialization state diagram .....                  | 105 |
| 10.5.4.7              | Slave Initialization state diagram.....                    | 110 |
| 10.5.4.8              | Slave AL_PA position map state diagram.....                | 113 |
| 10.5.4.9              | Master Initialization state diagram.....                   | 115 |
| 10.5.4.10             | Master AL_PA position map state .....                      | 117 |
| Annex A (normative)   | L_Port Elasticity buffer management .....                  | 119 |
| A.0                   | Overview .....   | 119 |
| A.1                   | L_Port elasticity buffer implementation.....               | 119 |
| A.2                   | Clock skew management .....                                | 119 |
| A.3                   | Clock skew management states .....                         | 120 |
| A.3.0                 | Clock skew overview .....                                  | 120 |
| A.3.1                 | Insertion pending .....                                    | 120 |
| A.3.2                 | Quiescent.....   | 120 |
| A.3.3                 | Deletion pending .....                                     | 120 |
| A.3.3.1               | Low priority deletion pending.....                         | 121 |
| A.3.3.2               | High priority deletion pending .....                       | 121 |
| A.4                   | Buffer size .....  | 122 |
| Annex B (informative) | Loop Port State Machine examples .....                     | 123 |
| B.0                   | Overview .....   | 123 |
| B.1                   | L_Port initialization example .....                        | 123 |
| B.2                   | N_Port Login example .....                                 | 124 |
| Annex C (informative) | Dynamic Half-Duplex.....                                   | 126 |
| C.0                   | DHD Overview.....  | 126 |
| C.1                   | Close initiative description .....                         | 126 |
| C.2                   | Dynamic Half-Duplex examples .....                         | 127 |
| Annex D (informative) | Access unfairness .....                                    | 128 |
| D.0                   | Overview .....   | 128 |
| D.1                   | Improving Loop performance .....                           | 128 |
| D.2                   | Emptying ACK .....   | 128 |
| Annex E (informative) | Half-duplex operation .....                                | 129 |
| Annex F (informative) | BB_Credit and Available_BB_Credit management example ..... | 130 |
|                       | L_Port A.....  | 130 |
|                       | L_Port B.....  | 130 |

|  |     |
|--|-----|
| Annex G (informative) L_Port clock design options.....                         | 132 |
| G.0Overview.....   | 132 |
| G.1L_Port synchronous clock design .....                                       | 132 |
| G.2L_Port asynchronous clock design .....                                      | 132 |
| G.3Clock skew management function periodicity.....                             | 133 |
| Annex H (informative) Mark synchronization examples.....                       | 134 |
| H.0Overview .....  | 134 |
| H.1Clock synchronization.....  | 134 |
| H.2Disk spindle synchronization.....   | 134 |
| Annex I (informative) Port Bypass Circuit example and usage.....               | 136 |
| I.0Overview.....   | 136 |
| I.1Port Bypass Circuit .....   | 136 |
| I.1.0Overview .....  | 136 |
| I.1.1Default bypass .....  | 137 |
| I.1.2Power-on reset bypass .....   | 137 |
| I.2Using a Port Bypass Circuit.....  | 137 |
| I.2.1Diagnostic Test of the Port Bypass Circuit .....                          | 137 |
| I.2.2Recovery from Loop Failure.....   | 138 |
| I.2.3Power-on with a failing L_Port .....                                      | 138 |
| I.2.4Reconfiguring a Loop with LPB and LPE.....                                | 138 |
| Annex J (informative) Public L_Ports and Private NL_Ports on a Loop .....      | 139 |
| Annex K (informative) Assigned Loop Identifier .....                           | 140 |
| Annex L (informative) Selective replicate for parallel query acceleration..... | 141 |
| L.0Overview.....   | 141 |
| L.1Parallel query technology .....   | 141 |
| L.2Shared disk cluster .....   | 142 |
| L.3Parallel query example.....   | 142 |
| Annex M (informative) Controlled FC-AL configurations .....                    | 145 |
| M.0Overview.....   | 145 |
| M.1Address Control .....   | 145 |
| M.1.0Overview .....  | 145 |
| M.1.1Preferred Hard Addressing .....   | 145 |
| M.1.2Required Hard Addressing.....   | 145 |
| M.2Configuration Change Control .....  | 146 |
| M.2.0Overview .....  | 146 |
| M.2.1Port Bypass Circuit Control.....  | 146 |
| M.2.2Loop Initialization Control .....   | 146 |
| Annex N (Informative) Insertion modes of Hubs .....                            | 147 |
| Annex O (informative) L_Port power-on considerations .....                     | 148 |
| Annex P (Informative) L_Port initialization flow diagram .....                 | 149 |
| Annex Q (informative) Examples of Switch Port Initialization .....             | 150 |
| Q.0Overview.....   | 150 |
| Q.1Example 1: two E/F/FL_Port-capable Switch .....                             | 150 |

|   |     |
|---|-----|
| Q.2Example 2: two E/F/FL_Port-capable Switch Ports and one Nx_Port .....      | 151 |
| Q.3Example 3: one E/F/FL_Port-capable Port and one E/F_Port-capable Port..... | 152 |
| Table 1 — 8B/10B characters with neutral disparity.....                       | 26  |
| Table 2 – Primitive Signals.....  | 28  |
| Table 3 — Primitive Sequences .....   | 28  |
| Table 4 — MONITORING (State 0) transitions .....                              | 63  |
| Table 5 — ARBITRATING (State 1) transitions .....                             | 67  |
| Table 6 — ARBITRATION WON (State 2) transitions .....                         | 70  |
| Table 7 — OPEN (State 3) transitions .....                                    | 72  |
| Table 8 — OPENED (State 4) transitions .....                                  | 74  |
| Table 9 — XMITTED CLOSE (State 5) transitions.....                            | 77  |
| Table 10 — RECEIVED CLOSE (State 6) transitions.....                          | 80  |
| Table 11 — TRANSFER (State 7) transitions .....                               | 83  |
| Table 12 — INITIALIZATION process (State 8) transitions .....                 | 85  |
| Table 13 — Reserved .....   | 85  |
| Table 14 — OLD-PORT (State A) transitions.....                                | 85  |
| Table 15 — AL_PA mapped to bit maps.....                                      | 91  |
| Table C.1 — Dynamic Half-Duplex.....  | 127 |
| Table K.1 — Assigned Loop Identifier .....                                    | 140 |

|  |     |
|--|-----|
| Figure 1 — Fibre channel roadmap .....                           | 10  |
| Figure 2 — Examples of the Loop topology .....                   | 21  |
| Figure 3 — FC-PH with Arbitrated Loop addition .....             | 23  |
| Figure 4 — State Diagram.....                                    | 44  |
| Figure 5 — Loop Initialization Sequences .....                   | 89  |
| Figure 6 — Loop Initialization Sequence AL_PA bit map .....      | 93  |
| Figure 7 — Loop Initialization state diagram example.....        | 97  |
| Figure 8 — POWER-ON state diagram .....                          | 100 |
| Figure 9 — OLD-PORT state diagram .....                          | 101 |
| Figure 10 — Loop Fail Initialization state diagram .....         | 103 |
| Figure 11 — Normal Initialization state diagram .....            | 105 |
| Figure 12 — OPEN-INIT state diagram .....                        | 107 |
| Figure 13 — Slave Initialization state diagram.....              | 110 |
| Figure 14 — Slave AL_PA position map state diagram.....          | 113 |
| Figure 15 — Master Initialization state diagram.....             | 115 |
| Figure 16 — Master AL_PA position map state diagram.....         | 117 |
| Figure A.1 — Elasticity buffer.....                              | 119 |
| Figure A.2 — Clock skew management states.....                   | 120 |
| Figure G.1 — Example of a synchronous L_Port design.....         | 132 |
| Figure G.2 — Example of an asynchronous L_Port design .....      | 132 |
| Figure I.1 — Example Port Bypass Circuit.....                    | 136 |
| Figure J.1 — Public L_Ports and Private NL_Ports on a Loop ..... | 139 |
| Figure L.1 — FC-AL parallel query server .....                   | 142 |
| Figure P.1 — L_Port initialization flow diagram .....            | 149 |
| Figure Q.1 — Switch Initialization example 1.....                | 150 |
| Figure Q.2 — Switch Initialization example 2.....                | 151 |
| Figure Q.3 — Switch Initialization example 3.....                | 152 |

## INFORMATION TECHNOLOGY – FIBRE CHANNEL –

### Part 122: Arbitrated loop-2 (FC-AL-2)

#### FOREWORD

- 1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards. Their preparation is entrusted to technical committees; any ISO and IEC member body interested in the subject dealt with may participate in this preparatory work. International governmental and non-governmental organizations liaising with ISO and IEC also participate in this preparation.
- 2) In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.
- 3) The formal decisions or agreements of IEC and ISO on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC and ISO member bodies.
- 4) IEC, ISO and ISO/IEC publications have the form of recommendations for international use and are accepted by IEC and ISO member bodies in that sense. While all reasonable efforts are made to ensure that the technical content of IEC, ISO and ISO/IEC publications is accurate, IEC or ISO cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 5) In order to promote international uniformity, IEC and ISO member bodies undertake to apply IEC, ISO and ISO/IEC publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any ISO/IEC publication and the corresponding national or regional publication should be clearly indicated in the latter.
- 6) ISO and IEC provide no marking procedure to indicate their approval and cannot be rendered responsible for any equipment declared to be in conformity with an ISO/IEC publication.
- 7) All users should ensure that they have the latest edition of this publication.
- 8) No liability shall attach to IEC or ISO or its directors, employees, servants or agents including individual experts and members of their technical committees and IEC or ISO member bodies for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication of, use of, or reliance upon, this ISO/IEC publication or any other IEC, ISO or ISO/IEC publications.
- 9) Attention is drawn to the normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 10) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

**This consolidated version of the official IEC Standard and its amendment has been prepared for user convenience.**

**ISO/IEC 14165-122 edition 1.1 contains the first edition (2005) and its Amendment 1 (2008).**

**A vertical line in the margin shows where the base publication has been modified by Amendment 1.**



International Standard ISO/IEC 14165-122 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

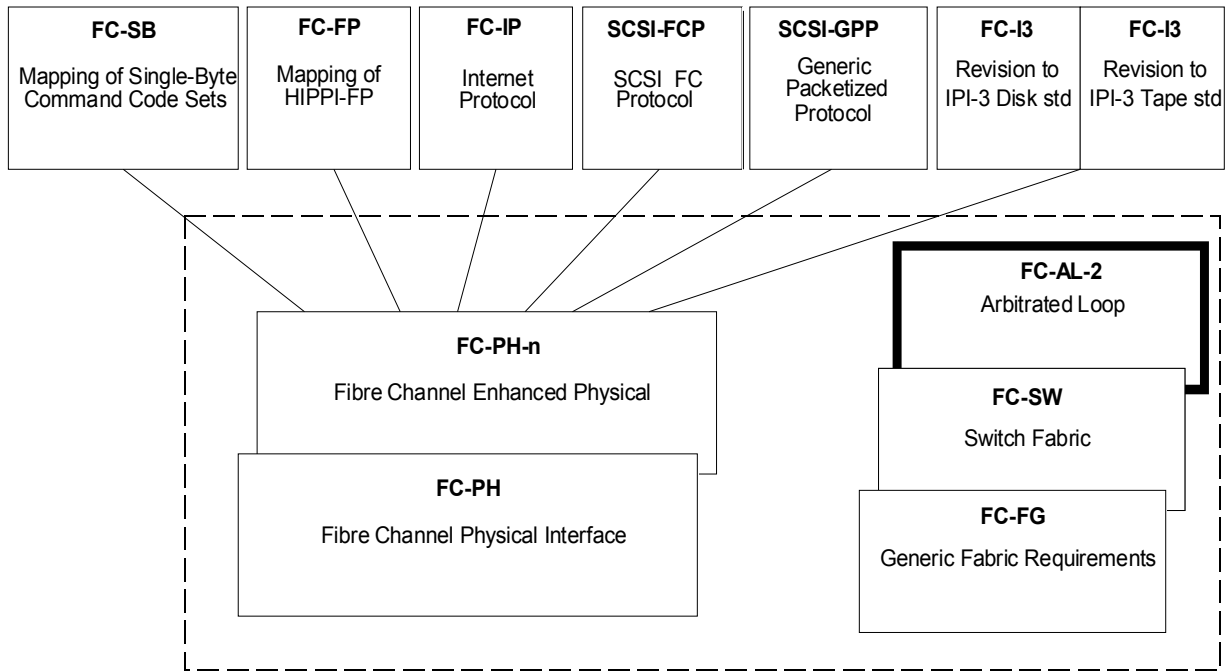
The list of all currently available parts of ISO/IEC 14165 series, under the general title *Information technology – Fibre channel*, can be found on the IEC web site.

This International Standard has been approved by vote of the member bodies, and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

## INTRODUCTION

International Standard ISO/IEC 14165-122 specifies an enhancement to the signaling protocol of the Fibre Channel Physical and Signaling Interface (FC-PH), ISO/IEC 14165-251, to support communication among two or more Ports without using the Fabric topology. The following diagram shows the relationship of this document to other parts of Fibre Channel. FC-PH-n refers to *n* versions of FC-PH. The roadmap is intended to show the general relationship of documents to one another, not a hierarchy, protocol stack or system architecture. It does not show the complete set of Fibre Channel documents.



**Figure 1 — Fibre channel roadmap**

FC-AL features enhanced Ports, called L\_Ports, which arbitrate to access an Arbitrated Loop. Once an L\_Port wins arbitration, a second L\_Port may be opened to complete a single point-to-point circuit (i.e., communication path between two L\_Ports). When the two connected L\_Ports release control of the Arbitrated Loop, another point-to-point circuit may be established. An L\_Port may have the ability to discover its environment and works properly, without outside intervention, with an F\_Port, an N\_Port or with other L\_Ports.

There is no change to the framing protocol of FC-PH-n, however, modification to the Port hardware is required to transmit, receive and interpret the new Arbitrated Loop Primitive Signals and Sequences.

## INTRODUCTION to Amendment 1

Since the publication of ISO/IEC 14165-122:2005 (FC-AL) important technical corrections have been developed.

FC-AL-2 defines a method for the operation of a FC arbitrated loop. This amendment revises the base document, FC-AL-2, with respect to some inconsistencies found since approval of the base document.

This amendment contains the following changes:

- the transmission word delay through an L\_Port is changed from 6 words to 12 words to accommodate higher fibre channel speeds; for example, 8 Gbit/s and 16 Gbit/s.
- the OPEN state is corrected to assure fairness for an L\_Port that is using the TRANSFER state while another L\_Port is using ARBf.

## INFORMATION TECHNOLOGY – FIBRE CHANNEL –

### Part 122: Arbitrated loop-2 (FC-AL-2)

#### 1 Scope

This part of ISO/IEC 14165 specifies signaling interface enhancements for FC-PH, to allow L\_Ports to operate with an Arbitrated Loop topology. This standard defines L\_Ports that retain the functionality of Ports as specified in FC-PH. The Arbitrated Loop topology attaches multiple communicating points in a loop without requiring switches.

The Arbitrated Loop topology is a distributed topology where each L\_Port includes the minimum necessary function to establish a Loop circuit. A single FL\_Port connected to an Arbitrated Loop allows multiple NL\_Ports to attach to a Fabric.

When an L\_Port is operating on a Loop with at least one other L\_Port, the L\_Port uses the protocol extensions to FC-PH that are specified in this standard.

When an L\_Port is connected with an N\_Port or an F\_Port, the L\_Port communicates using the protocol defined in FC-PH.

Each L\_Port may use a self-discovering procedure to find the correct operating mode without the need for external controls.

#### 2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 14165-131, *Information technology — Fibre Channel — Part 131: Switch Fabric Requirements (FC-SW)*

ISO/IEC 14165-141, *Information technology — Fibre Channel — Part 141: Fabric Generic Requirements (FC-FG)*

ISO/IEC 14165-251, *Information technology — Fibre Channel — Part 251: Framing and Signaling (FC-FS)*<sup>1</sup>

INCITS 230:1994 [R2004], *Fibre Channel — Physical and Signaling Interface (FC-PH) [T11]*

Amendment 1 (1996)

Amendment 2 (1999)

<sup>1</sup> Under consideration.